Morphological Co-Processing Unit for Embedded Devices

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Abstract This paper focuses on the development of a fully programmable morphological coprocessor for embedded devices. It is a well-known fact that the majority of morphological processing operations are composed of a (potentially large) number of sequential elementary operators. At the same time, the industrial context induces a high demand on robustness and decision liability that makes the application even more demanding. Recent stationary platforms (PC, GPU, clusters) no more represent a computational bottleneck in real-time vision or image processing applications. However, in embedded solutions such applications still hit computational limits.

The Morphological Co-Processing Unit (MCPU) replies to this demand. It combines the previously published efficient dilation and erosion units with geodesic units to support a larger collection of morphological operations, from a simple dilation to a pattern spectrum by reconstruction.

The coprocessor has been integrated into a FPGA platform running a server, able to respond client's requests over the ethernet. The experimental performance of the MCPU measured on a wide set of operations brings as results in orders of magnitude better than another embedded platform an ARM A9 quad-core processor.

Keywords Mathematical Morphology, Hardware Implementation, Pattern Spectrum, Reconstruction, Parallel Computation

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1 Introduction

Mathematical morphology is an image processing framework providing a complete set of tools for filtering, multiscale image analysis, or pattern recognition. It is used in a number of applications, including biomedical and medical imaging, video surveillance, industrial control, video compression, stereology or remote sensing since its very first appearance in the late 1960's, see [18, 24–26].

Considering the hardware implementation context, several different trends have been observed. A recent technological advance of imaging sensors stimulated the development of applications by means of high-resolution images that became a standard. Needless to say large images impose challenging requirements on the computation platform in terms of both performance and memory.

On the other hand, the industrial context often induces severe real-time constraints on applications. Often these demanding image-interpretation applications require a high correct-decision liability, robust but costly multi-criteria and/or multi-scale analyses are used. Given that image processing should not deteriorate industrial productivity, the latency and computational performance are of high interest in this context.

In embedded systems, the most important concerns are low power consumption (and consequently low heat dissipation) and small resources occupation, which allows for better embedding. All these considerations combined together infer overwhelming requirements on the architecture of polyvalent processing units addressing many different contexts. The context of embedded morphology applications includes, for instance, an augmented vision system that improves visual perception [10], or smart cameras [13].

The paper is organized as follows: Section 2 makes a short survey of existing morphological algorithms and architectures. Section 3 outlines the basic definitions of typical mathematical morphology operations. Section 4 describes how these operations can be efficiently computed by processing pipelines and describes the architecture of the proposed coprocessor. The following Section 5 covers the pro-

grammability and user interface to the coprocessor server. Finally, Section 6 presents experimental results obtained on an FPGA board and compares them to an ARM A9 embedded platform.

2 State of the art

This section briefly presents the state of the art algorithms for elementary morphology operations dilation and erosion and their hardware implementations in FPGA. The last part discusses the novelty and main contributions of this paper.

2.1 Algorithms

The simplest method to compute a dilation is the exhaustive search for maximum in the scope of SE B according to the definition below in Eq. 1. This naive solution tends to need a large number of comparisons, which are on most platforms diadic (with two operands). The number of comparisons is considered as a metric of algorithm complexity, so the naive algorithm has complexity $\mathcal{O}(l)$ as it has to carry out $l-1$ comparisons for a SE containing l pixels. Such complexity suggests that the naive algorithm is inefficient for large SEs. Pecht [22] proposed a method to decrease the complexity based on the logarithmic SE decomposition, thereby achieving $\mathcal{O}(\lceil \log_2(l) \rceil)$ complexity.

The first 1-D algorithm that reduced complexity to a constant is often referred to as HGW (it was published simultaneously in two papers: van Herk [31], and Gil and Werman [12]). The computation complexity is constant, i.e., of $\mathcal{O}(1)$, which means the upper bound of the computation time is independent of the SE size. Gil [11] proposed an improved version of HGW that lowered the number of comparisons per element, but at the cost of increased memory usage and implementation complexity.

Lemire [15] proposed a fast stream algorithm of $\mathcal{O}(1)$ for causal line SEs. This algorithm uses two queues of length l in order to store the pixels that form locally monotonous signal (i.e., monotonously increasing and decreasing). Although it produces both erosion and dilation simultaneously, it works with causal SEs only. This downside was solved later by Dokladal [8] who proposed another queue-based algorithm. The advantages of these queue-based algorithms are strictly sequential access to data, zero latency, and low memory requirements.

The 2-D dilation is usually obtained by composition of 1-D dilations, see for instance Soille [28] who approximates circle and polygon SEs using rotated line SEs. However, this technique covers only a limited family of shapes. The arbitrary-shaped SE are obtained by either more complex 2-D algorithms (e.g., Urbach [30]), which are suitable for general-purpose processors, or by fine-grained decomposition of the large SE into a set of small 2-D SEs. Xu [34] proposed that any 8-convex polygon (convex on 8-connectivity grid, hence 8-convex) is decomposable into a class of 13 nontrivial indecomposable convex polygonal SEs. Normand [20] reduced the class of shapes to only four 2-pixel SEs by allowing the union operator to take place in the SE decomposition.

2.2 Hardware implementations

One of the first morphology architectures was the texture analyzer by Klein [14]. It was optimized for linear and rectangular SE by decomposition into line segments. More recently, Velten [32] proposed another, delay-line based architecture for binary images supporting arbitrarily shaped 3×3 SEs. The computation of dilation is realized by OR gates (topology was not communicated, probably a tree of diadic OR gates) achieving good performance, which was further improved by spatial parallelism.

Clienti [4] proposed a highly parallel morphological System-on-Chip. It is a set of neighborhood processors optimized for arbitrarily shaped 3×3 SE interconnected in a partially configurable pipeline. Each stage of the pipeline contains 2 processors that can process 2 parallel image streams and an ALU. The reconfiguration allows all the processors to be connected in one chain in order to employ all processors when only one image stream is used. A reconfigurable 3x3 neighborhood morpho processor was recently used in Gibson [10] in a hand-held augmented-vision system for visually impaired.

Another approach is called partial-result reuse (PRR). The morphological operation by some neighborhood B_1 in an early stage is delayed by delay lines in order to be reused later in computation by some other neighborhood B_2 obtaining larger B_3 decreasing thus the number of necessary comparisons. One of the first PRR architectures for 1-D dilation was proposed in [23] and improved in [6]. The principle is based on an exponential growth of the intermediate neighborhoods in the partial-result reuse scheme.

Chien [3] presented more general concept of PRR that builds the desired SE by a set of distinct partial neighborhoods computed by a dedicated algorithm. As a result, it supports arbitrary 8-convex polygon at the cost of some additional comparisons.

A similar approach has been published by Déforges [7]. Based on the [20] SE decomposition (a SE is decomposed into a number of causal 2-pixel SEs, which are applied in sequence or in parallel and combined with a stream implementation, the authors proposed a methodology for pipeline architecture design supporting arbitrary convex SEs.

Recently, Torres-Huitzil [29] designed a linear systolic-like array of processing elements without need for delay-line internal memory storage supporting non-rectangular flat SEs. However, prospective drawbacks can be seen in the chosen column-based image scan requiring significant image storage capability, and the need of deep parallelism to attain real-time performance even for the mentioned 7×7 SE.

The last method mentioned in this overview is the implementation of efficient 1-D algorithms. To our knowledge,

there are only few such contributions in the literature. Clienti [5] published architectures for the 1-D Lemonier algorithm [16] and the HGW algorithm. Both architectures however suffers from the necessity of forward and reverse image scans imposed by algorithms, which increases memory requirements by additional buffers.

Recently, Bartovsky [1] proposed implementation of the Dokladal algorithm [8] as a processing unit by polygonal SEs with a strictly sequential access to data and small memory requirements. This architecture is mainly beneficial for large SEs because only the memory varies with the size of the SE, the computation logic remains the same.

3 Basic notions

This section describes the operators used in this paper. We are mainly interested in compound operators composed as concatenations of elementary operators, that are therefore costly on sequential machines.

Let δ_B, ε_B: $\mathbb{Z}^2 \to \mathbb{R}$ be a dilation and an erosion on gray-scale images, parameterized by a structuring element B, assumed to be flat (i.e., $B \subset \mathbb{Z}^2$) and translation-invariant, defined as [24, 27]

$$\delta_B(f) = \bigvee_{b \in B} f_b \; ; \qquad \varepsilon_B(f) = \bigwedge_{b \in \widehat{B}} f_b \tag{1}$$

where f_b denotes translation of f by b. The hat $\widehat{\ }$ denotes the transposition of B, equal to the set reflection $\widehat{B} = \{x \mid -x \in B\}$.

The concatenation of dilation and erosion forms other morphological operators. The closing and opening on gray-scale images, φ_B, γ_B: $\mathbb{Z}^2 \to \mathbb{R}$, parameterized by a structuring element B, are defined as

$$\varphi_B(f) = \varepsilon_B[\delta_B(f)] \; ; \qquad \gamma_B(f) = \delta_B[\varepsilon_B(f)] \tag{2}$$

Closing and opening are filters. Their concatenation forms alternating filters $\gamma\varphi$, $\varphi\gamma$, $\gamma\varphi\gamma$ and $\varphi\gamma\varphi$. Other filters can be obtained by combining *families* of filters. A well known example is the alternating sequential filter (ASF), composed as sequence of closings and openings with a progressively increasing SE λB, with $\lambda > 0$. Let γ^λ and φ^λ denote the change of scale such as $\gamma_{\lambda B}$ and $\varphi_{\lambda B}$. Then λ-order ASF (referred to as ASF$^\lambda$) is composed as

$$\text{ASF}^\lambda = \varphi^\lambda \gamma^\lambda \varphi^{\lambda-1} \gamma^{\lambda-1} \dots \varphi^1 \gamma^1 \tag{3}$$

starting with opening, and

$$\text{ASF}^\lambda = \gamma^\lambda \varphi^\lambda \gamma^{\lambda-1} \varphi^{\lambda-1} \dots \gamma^1 \varphi^1 \tag{4}$$

starting with closing.

Let $\delta_f : \mathbb{Z}^2 \to \mathbb{R}$ be an elementary geodesic dilation of image g (marker) "under" image f (mask) where $g \leq f$, such as [33]

$$\delta_f(g) = f \wedge \delta_{3\times3}(g) \tag{5}$$

Repeating $\delta_f(f)$ until stability represents the dilation-reconstruction of g under f; $g \leq f$,

$$\rho_f(g) = \underbrace{\delta_f \delta_f \dots \delta_f}_{x \text{ times}}(g) \tag{6}$$

the number of iterations $x = \infty$ by definition, and practically until the idempotence. The marker image g is commonly obtained by morphological opening γ_B. In this case, the operation is called opening by reconstruction γ^ρ_B, defined as

$$\gamma^\rho_B(f) = \rho_f(\gamma_B(f)) \tag{7}$$

Let $\{\gamma^{\lambda_i}\}$, with $\lambda_i > \lambda_{i-1}$ and with $\lambda_i > 0$, $\forall i$ be a collection of openings, generating a size distribution aka granulometric function (see Matherons' axioms, [18] p. 192) using some measure, e.g. integral (or sum) of the image. One also often uses its derivative, so called granulometric or pattern spectrum, defined as

$$PS_{\lambda_j B}(f) = \sum_D \left(\gamma_{\lambda_i B} f - \gamma_{\lambda_j B} f\right) \tag{8}$$

with $D = \text{spt}(f)$. Notice, that instead of opening $\gamma_{\lambda_i B}$ one also may want to use the opening by reconstruction $\gamma^\rho_{\lambda_i B}$ which even more increases the computation cost.

4 Hardware architecture

This section describes the hardware architecture of the proposed morphological coprocessor that efficiently implements the aforementioned sequential, costly operators. The following description follows the bottom-up approach, so we start with developing two basic image processing pipelines, one for large SE operators, and one for geodesic operators. Then we build the processing core by surrounding these two pipelines with interconnection busses, configuration registers, and image buffers in such way that it can be used as a peripheral of the Xilinx MicroBlaze. Finally, we describe the top-level architecture of the FPGA evaluation platform.

4.1 Large SE Pipeline

Let us begin with the description of the Large SE pipeline.

One of the most penalizing aspects in morphological operators is the number of iteration on an image. On sequential platforms, this induces an intensive traffic between the CPU and the memory. An important efficiency can be obtained when such iterations can be pipelined. This idea is used in Clienti [5]. However, given that its pipeline is only composed of 3×3 blocks it lacks flexibility and must be reconfigured to precisely fit application needs.

In this paper, in order to gain in flexibility we propose two parallel pipelines of programmable large-size SE units. To efficiently execute the largest collection of operators (including those with two parallel branches, such as top hat or

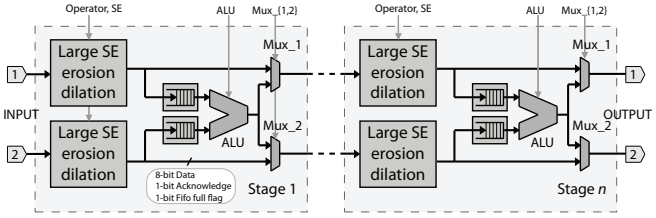

Fig. 1 Large SE pipeline architecture.

gradient) the pipelines are interconnected by programmable ALUs (Arithmetic Logic Unit), see Fig. 1.

Either pipeline contains several identical parts called processing stages connected one after the other. The pipeline is scalable by means of the number of instantiated stages, which is hereafter denoted as n. A common number for Virtex-5 FPGA may be 4 to 5. The heart of each stage is a pair of Large SE erosion/dilation units. The output of both units can be connected to the ALU, or directly to the next stage through the Mux_$\{1,2\}$ multiplexer. The ALU result can be routed to either input port of the next stage (or both.

The Large SE erosion/dilation unit performs one morphological dilation or erosion by a flat rectangular or octagonal SE of programmable size (up to 31 pixels in diameter for rectangles and 43 pixels in diameter for octagons) and the position of the origin. This unit takes advantage of separability of 2-D rectangular and octagonal SEs into a sequence of 1-D SEs. The 1-D dilation is then computed by a queue-based algorithm [8], the FPGA implementation of which has been proven to be beneficial for high-demanding image processing with large SEs. The description of the FPGA architecture and experimental results can be found in [2] for rectangle SEs, and [1] for octagon SEs, respectively.

The previously published results can be summarized as follows. The Large SE unit computes 2-D rectangular or octagonal erosion/dilation during a single horizontal image scan with minimal latency. The experimentally obtained average processing rate is approximately 2.5 clock cycles per pixel, i.e., approx. 50 Mpx/s at 125 MHz clock frequency. The memory requirement is another important parameter of an image processing implementation because it limits the number of units that fit the FPGA. The most significant memory requirement of the Large SE unit is given by the set of queues, such as

$$R = NH \times (bpp + \lceil \log_2(H-1) \rceil) \text{ [bits]} \qquad (9)$$

where N denotes image width, H the height of the SE, bpp the number of bits per pixel, and $\lceil . \rceil$ the ceiling operation. For example, let $N = 1024$ px, $H = 31$ px, and $bpp = 8$ bits. The memory requirement is then

$$R = 31744 \times 13 \text{ [bits]} \qquad (10)$$

The dilation/erosion computation can be turned off by a bypass feature. Then the computation memory changes into a large FIFO buffer that can be used to synchronize dataflows in two-channel operations, such as top-hat, gradient etc.

The ALU performs simple arithmetic operations of two pixels, each of which can be configured as either ALU input image streams or a programmable constant. The supported operations are as follows: no operation; negation (logical complement); bit-wise AND, OR, XOR; saturated addition, subtraction; infimum and supremum. In order to ensure that the ALU has both input pixels at the same coordinates in respective images, the both image streams have to be synchronized within some tolerance provided by FIFO memories. In the case that either FIFO is empty, the ALU is stalled.

The Measurement unit computes simple metrics of the whole image, namely the sum, infimum, and supremum. This measurement is useful in image analysis applications, such as pattern spectrum, and can be obtained on-the-fly at a low cost. The measurement results can be read out through the configuration registers.

All programmable parameters including the SE dimensions, operation, multiplexers and ALU settings, as well as measurement results, are stored in a bank of per-stage configuration registers.

4.2 Geodesic pipeline

A significant subset of morphological operators relies on the reconstruction using the geodesic dilation/erosion by 3×3 SE. Even though the Large SE pipeline supports geodesic operations, using it would be inefficient. A better solution is to devise a dedicated Geodesic pipeline, see Fig. 2.

This Geodesic pipeline contains several equal stages connected one after another. The pipeline is scalable by means of the number of stages instantiated, which is hereafter denoted as m (e.g., $m = 16$ for Virtex 5). The heart of each stage is a 3×3 erosion/dilation unit. The output of this unit is connected to the ALU, along with the buffered Mask image. The ALU result is the Marker input of the next stage.

The 3×3 dilation is outlined in Fig. 3. It also takes advantage of separability of the rectangle into the horizontal and vertical segments, which are implemented using a well-known approach of delay elements (registers T for horizontal segment, and line buffers xT for vertical segments) and comparators. This approach is suitable for small-sized SEs and delivers better FPGA area and performance results than the queue-based architecture (which are better for large SEs).

The ALU is the same as described above. The reason for the Line buffer is to synchronize the Mask image and the dilated Marker image, which is delayed by $N+1$ pixels (recall N is the width of the image).

4.3 Morphological Co-Processor Unit (MCPU) Schematics

The MCPU architecture in Fig. 4 is composed of the two processing pipelines surrounded by a set of image stream routing multiplexers, configuration registers, and image buffers. The multiplexers allow two input and two output

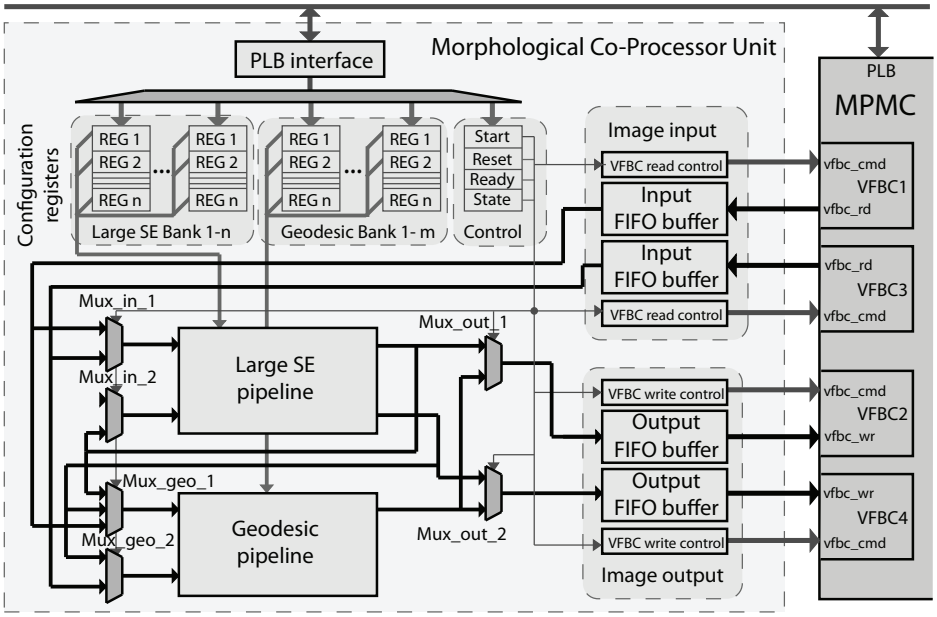

Fig. 4 Architecture of the Morphological Co-Processor Unit. Black line denotes an image data bus, grey line denotes configuration and control.

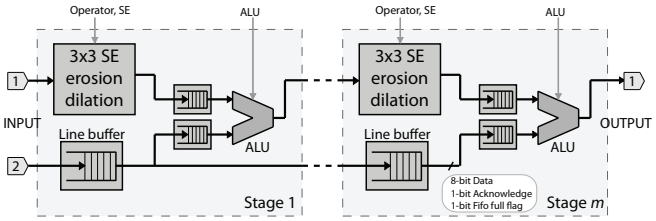

Fig. 2 Geodesic pipeline architecture.

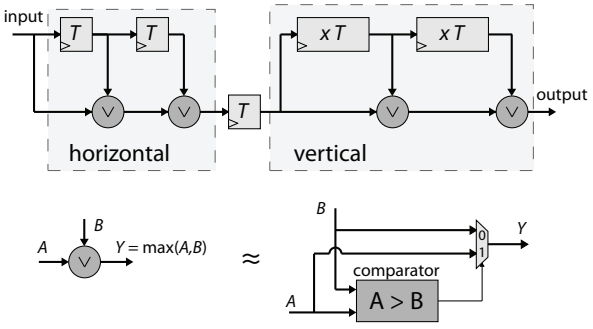

Fig. 3 3×3 dilation unit for the geodesic pipeline.

image streams to be routed to the pipelines in different configurations (serial, parallel, see Fig. 6) as described later in Sec. 5.

The configuration registers store the necessary configuration for all the processing units in both pipelines, the global control, and measurement results. Notice that there is one bank of registers for each stage of the processing pipelines.

Image data are transferred by 4 VFBC channels, two VFBC channels are dedicated to reading input image data from the DDR2 memory, and other two for writing the output image data to the DDR2 memory. The image transfers are independent of each other, so the processing can run in-place (the output image is written in place of the input image). The VFBC allows us to read and/or write image data to the DDR memory with a FIFO-like data-flow control (full, almost full, empty, almost empty flags), so the data stream can be stalled by either endpoint if necessary. The image data in both directions are buffered in Input or Output buffers, respectively.

The MCPU is intended to be used as a peripheral in a higher-level environment. We have tested it as a peripheral of the Xilinx MicroBlaze as described in the following section.

4.4 Top-level architecture

An example of a top-level architecture, we have built for evaluation purposes, is outlined in Fig. 5. The proposed MCPU is a coprocessor running as a peripheral of the MicroBlaze CPU synthesized on a Virtex 5 development platform. This platform is also provided with an ethernet link. The architecture consists of two main parts: (i) the MCPU core, and (ii) the MicroBlaze processor environment.

This platform plays several roles: i) the MicroBlaze configures and sends operators to MCPU to execute, ii) provides working memory storage capacity, and iii) handles the communication with the outside world.

A very important aspect of every image processing platform is the memory for storing images; either input, output, or intermediate result. The MCPU uses the Xilinx proprietary Multi-Port Memory Controller MPMC that provides a multi-port interface to a high-capacity off-chip DDR2 memory. The MPMC is capable of handling 4 simultaneous im-

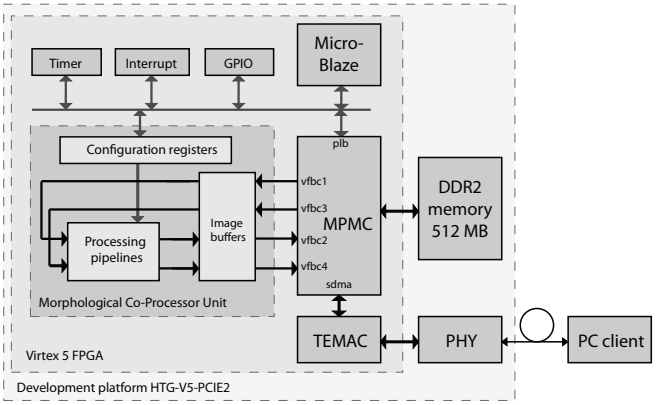

Fig. 5 Overall Platform architecture. Black line denotes image data transfers, grey line denotes configuration and control.

age data streams of approx. 50 Mpx/s each that are required by the processing core to sustain the maximal performance.

The MicroBlaze processor uses the Peripheral Local Bus (PLB) to control all the peripherals and to transfer the configuration data, which are small in size, among the peripherals.

5 User interface - programmability

The platform can be accessed via a tri-speed Ethernet interface using either TCP/IP or UDP/IP protocols (implemented as lightweight lwIp). The MCPU runs a server able to accept images and operations to execute via the ethernet link from a superior client.

In order to achieve a proper function of the MCPU server, the client has to manage the following tasks: communicate properly with MicroBlaze, send the image data, configure and run the processing core, read the results. The low-level implementation of these tasks being cumbersome, we have provided MCPU with C++ and Python interface (integrated in MorphM [19]). The interface contains two configuration approaches: (i) high-level, and (ii) low-level. The high-level configuration (built on the top of the low-level approach) provides more intuitive way to perform common morphological operators. The low-level configuration allows advanced users to better fit unusual applications to the processing pipeline. In the rest of this paper, we will discuss the high-level configuration only.

The list of supported operators includes dilation, erosion, opening, closing, reconstruction, opening and closing by reconstruction, top hat, gradient, ASF$^\lambda$, pattern spectrum, and pattern spectrum by reconstruction. All these operators proceed in the following steps: send the image (if necessary), calculate the configuration based on the passed arguments (either SE or λ), execute the processing pipelines, and read the output image and/or measurement results. Notice that operators with large values of SE or λ may not fit into the pipelines. In this case, several iteration are automatically executed. This is especially true for the reconstruction that may need hundreds of iterations.

The configuration encompasses: i) the configuration of processing units (namely the SE size and the operator) and ii) the interconnection using global and pipeline multiplexers. All operators can use one from the following 4 typical interconnection patterns depicted in Fig. 6. The most frequently used interconnection pattern is the one in Fig. 6(b) that connects all the Large SE units into a single long pipeline, which allows for very long concatenations of erosions and dilations in a single run.

5.1 Example: pattern spectrum

In this section, we show how the pattern spectrum operator is executed by the MCPU. The pattern spectrum $PS_{\lambda B}$ is a derivative of the granulometric function parameterized by the size λ and by the shape of the SE B, see Eq. 8. The single $PS_{\lambda B}$ suggests that number of increasing-size openings on the input image are required. However, according to the absorption law of filters (that obviously apply to openings)

$$\gamma^k = \gamma^k \gamma^l; \quad k > l > 0, \tag{11}$$

it is not necessary to compute each opening from the input image, as in Eq. 8. Instead, we can use the result of a previous opening. This allows chaining all large SE units into an efficient pipeline computing a number of openings at the same time during a single (or a few) image scans. Another advantage, over the pipeline of elementary dilation/erosion blocks (as e.g. in [4]), is the possibility of programming directly the sizes of the openings in the sequence since granulometries are often computed for application-specific, chosen values.

Figure 7 shows an example of execution of $PS_{\lambda B}$ for $n = 4$, $\lambda = 9$. Using the pipeline interconnection pattern, all 8 processing units are connected into a single chain. Considering that each unit supports SE up to 31×31, each opening requires just two processing units. Hence the processing executes 4 openings by increasing SE size, from 3×3 to 9×9, during the first iteration. When the computation is done, the sum measurement results from the even units represent the granulometric distribution function $\sum(\gamma_{kB}(f)); k = \{1, 2, 3, 4\}$. These values are retrieved and stored by the MicroBlaze. The other openings, from 11×11 to 19×19, are computed during the second iteration. The resulting $PS_{\lambda B}$ is obtained as by differentiation (subtraction two by two) of the granulometric distribution.

6 Experimental results

The proposed MCPU architecture has been implemented in VHDL and targeted to the Xilinx FPGA Virtex-5 development platform (XC5SLX95T) for demonstration purposes. Two different setups were implemented with such parameters to fully utilize the available FPGA resources and keep

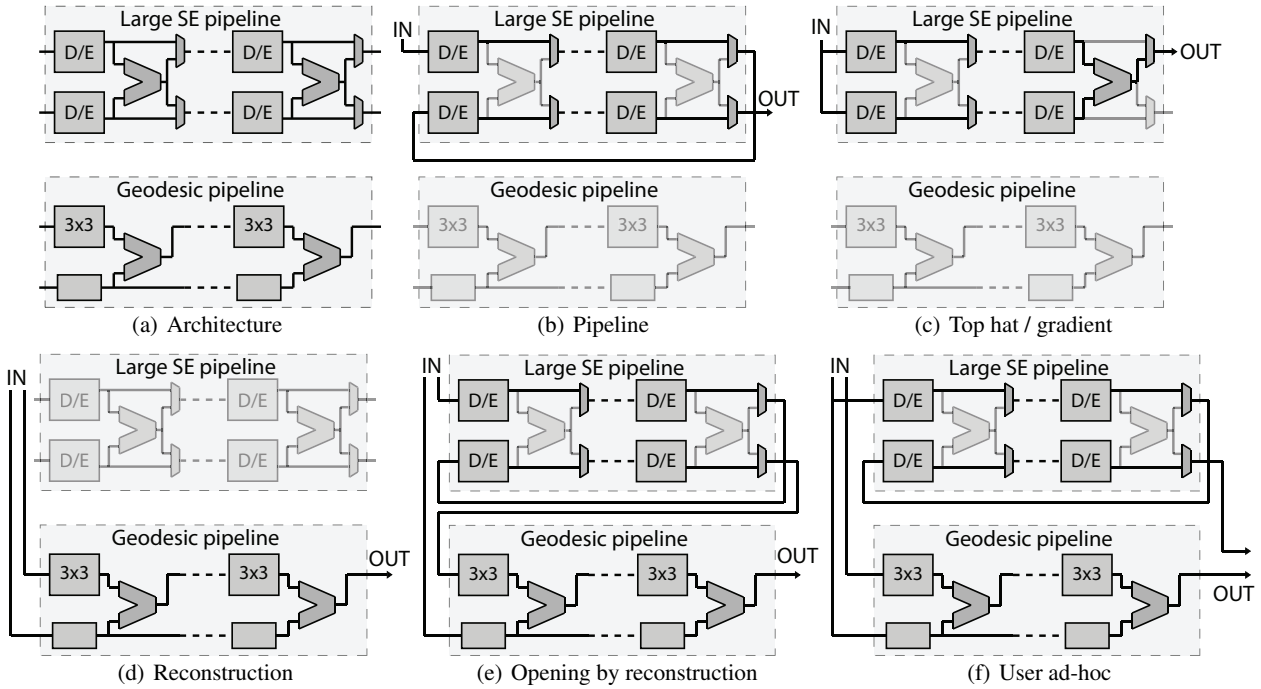

Fig. 6 Interconnection patterns of the Large SE and Geodesic pipelines.

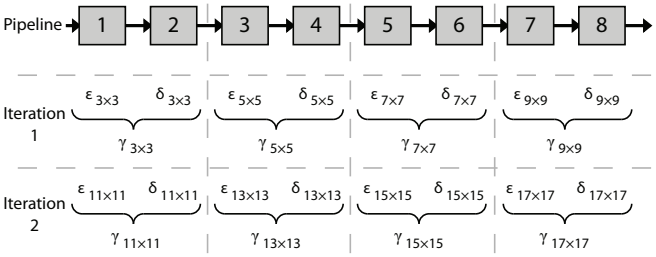

Fig. 7 Execution of the pattern spectrum operator, given $\lambda = 9, n = 4$

high flexibility at the same time. The implementation results and setup specification are outlined in Table 1.

Table 1 Implementation results

Parameter	Setup 1	Setup 2
Supported SE per unit	Rectangle 31×31	Octagon 43×43
Large SE stages n	5	4
Geodesic stages m	16	16
Image width N	1024	1000
FPGA Slice	13534	14684
FPGA BRAM	233	243
Clock frequency	125 MHz	125 MHz

We compare the performance of the proposed architecture against another embedded solution, an ARM processor. In our case, we use the Sabre platform [9] by Freescale, which can be seen as another example of handheld platform. The Sabre uses quad-core ARM A9 processor at 1GHz, 1GB of DDR3 memory up to 533MHz, and runs Linux with TCP/IP stack. We have created the benchmarks for two image processing libraries: (i) the well-known OpenCV [21], and (ii) more efficient Smil [17]. For the sake of completeness, we have also included the single-thread results of the OpenCV at desktop PC Intel Xeon running Linux.

The benchmark in Table 2 includes a set of aforementioned morphological operators on natural gray-scale photos 1000×1000 px. It includes an elementary 3×3 dilation, large opening and opening by reconstruction, alternating sequential filter, pattern spectrum and pattern spectrum by reconstruction. Apart from the 3×3 dilation, the common property of all these operators is the large number of operations, which is even undetermined for the reconstruction, and therefore, a high cost.

The experimental results show that the proposed MCPU architecture delivers performance by orders of magnitude superior to that of the Sabre platform, and even comparable with a desktop PC, for all high-cost operations, i.e., all in Table 2 but the 3×3 dilation. MCPU outperforms the other platforms (or is at least equivalent) whereever a high number of operators are sequentially applied to the image. Such a significant speed-up is allowed by possibility to thoroughly exploit the inter-operator parallelism via the pipelined computation. This is especially true for the opening and pattern spectrum by reconstruction when $m = 16$ geodesic dilations are computed at the same time. The speed-up becomes less significant for simple operators with small SEs, the performance for 3×3 dilation is worse than that of Smil at Sabre. This is due to a much higher clock of the ARM and the Xeon processors (1GHz and 2.7 Ghz, respectively). However, the

Table 2 Performance results of selected operators. Image is natural photo 1000×1000 px, time results are in milliseconds (unless seconds are specified).

Operator	Shape of SE	Size of SE or λ	MCPU	OpenCV at Sabre	Smil at Sabre	OpenCV at Xeon
Dilation	Rectangle	3×3	21.9	32.7	8.4	0.58
Opening	Rectangle	151×151	24.3	2450	1083	38.6
Opening	Octagon	151×151	41.9	246 s	2453	2301
Opening by recon.	Rectangle	151×151	544	47.6 s	22.1 s / 2110*	1940
Opening by recon.	Octagon	151×151	512	289 s	21.1 s	4356
ASF	Rectangle	$\lambda = 11$	64.2	4530	1987	57.1
ASF	Octagon	$\lambda = 11$	83.3	77 s	3872	814
Pattern spectrum *PS*	Rectangle	$\lambda = 11$	62.3	2570	1098	53.8
Pattern spectrum *PS*	Octagon	$\lambda = 11$	62.7	21.2 s	1782	249
PS by recon.	Rectangle	$\lambda = 11$	2530	190 s	85.3 s / 18.2 s*	8920
PS by recon.	Octagon	$\lambda = 11$	2410	201 s	81.5 s	8751

note *: The second result is obtained by an algorithm based on hierarchy queues.

majority of applications of mathematical morphology need a long sequence of operators that take advantage of the proposed parallelism.

7 Conclusions

This paper proposes a novel programmable morphological coprocessor for embedded devices based on FPGA devices. We have integrated previously published efficient dilation/erosion processing units and geodesic units into a MicroBlaze platform, which provides DDR memory storage and Ethernet connectivity, and thus created a very powerful coprocessor that supports a wide range of operators from a simple dilation to the pattern spectrum by reconstruction.

The coprocessor was experimentally evaluated at a Virtex5 development kit and compared to the quad-core ARM9 Sabre platform by Freescale running OpenCV and Smil libraries. The performance results for various compound operators (except the 3×3 dilation) shows a significant speed-up of at least one order of magnitude. The results of MCPU do even compare to that of a Xeon desktop workstation.

The future work will be focused on development of a compiler for MCPU that will automatically map a given application to the architecture. The current interface provides a user with a high-level programming interface. In the future, this compiler shall optimize the execution of concurrent operators, branching and simultaneous co-execution of an application on MCPU and the client.

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